WHAT IS CLAIMED IS:

1. A process for forming an interconnect comprising the steps of:

forming a lower interlayer dielectric over a semiconductor workpiece;

forming an interconnect metallization layer over the lower interlayer dielectric;

patterning a photoresist mask over the interconnect metallization layer, the photoresist including a masked region having a critical dimension and excluding an unmasked region;

etching the interconnect metallization layer in the unmasked region to leave a first metal line separated from a second metal line by an inter-line region, a width of the first and second metal lines corresponding to the critical dimension, the first and second metal lines exhibiting a parasitic capacitance;

forming a conformal middle interlayer dielectric over the first and second metal lines and over the lower interlayer dielectric in the inter-line region; and

forming a third metal line over the conformal middle interlayer dielectric, the third metal line electronically linked with the first metal line and projecting between the first and second metal lines in the inter-line region to elevate the parasitic capacitance and thereby reduce an overall variation in parasitic capacitance over a range of critical dimensions.

2. A process according to claim 1 wherein the interconnect metallization layer has a thickness, and

wherein the step of forming the middle interlayer dielectric comprises forming the middle interlayer dielectric with a thickness approximately 20% that of the interconnect metallization layer.

3. A process according to claim 1 wherein the step of forming the interconnect metallization layer comprises forming a layer composed substantially of aluminum.

4. A process according to claim 1 wherein the step of forming the middle interlayer dielectric comprises forming a layer selected from the group consisting of chemical vapor deposited oxide, borophosphosilicate glass, and tetraethylorthosilicate.

5. A process for forming an interconnect comprising the steps of:

forming a lower interlayer dielectric over a semiconductor workpiece;

patterning a photoresist mask over the lower interlayer dielectric, the photoresist including a masked region having a critical dimension and excluding an unmasked region;

etching the interlayer dielectric in the unmasked region to leave a first trench separated from a second trench by an inter-line region composed of the first interlayer dielectric, a width of the first and second trenches corresponding to the critical dimension;

forming an interconnect metallization layer over the lower interlayer dielectric and within the first and second trenches;

removing the interconnect metallization layer outside of the first and second trenches to leave a first metal line occupying the first trench and a second metal line occupying the second trench, the first and second metal lines exhibiting a parasitic capacitance;

removing the first interlayer dielectric in the inter-line region;

forming a conformal middle interlayer dielectric over the first and second metal lines and within the inter-line region; and

forming a third metal line over the conformal middle interlayer dielectric, the third metal line electronically linked with the first metal line and projecting between the first and second metal lines in the inter-line region to elevate the parasitic capacitance and thereby reduce an overall variation in parasitic capacitance over a range of critical dimensions.

6. A process according to claim 5 wherein the interconnect metallization layer has a thickness, and wherein the step of forming the middle interlayer dielectric comprises forming the middle interlayer dielectric with a thickness approximately 20% that of the interconnect metallization layer.

7. A process according to claim 5 wherein the step of forming the interconnect metallization layer comprises forming a layer composed substantially of copper.

8. A process according to claim 5 wherein the step of forming the middle interlayer dielectric

comprises forming a layer selected from the group consisting of chemical vapor deposited oxide, borophosphosilicate glass, and tetraethylorthosilicate.

9. In a process for forming an interconnect including the steps of patterning a photoresist mask featuring masked areas corresponding to a critical dimension, and then etching an underlying interconnect metallization layer in unmasked areas to leave adjacent first and second metal lines having a width corresponding to the critical dimension, a method for reducing variation in parasitic capacitance between the metal lines attributable to a variation in critical dimension, the method comprising the steps of:

determining a range of critical dimensions exhibited by a photolithography process; and

simulating variation in parasitic capacitance over the critical dimension range by determining the extent of penetration of an overlying third metal line into an inter-line region between the metal lines, a width of the inter-line region determined by a thickness of the conformal middle interlayer dielectric and by the critical dimension, such that penetration of the third metal line elevates parasitic capacitance while reducing parasitic capacitance variation over the critical dimension range.

10. In a process for forming an interconnect including the steps of patterning a photoresist mask featuring masked areas corresponding to a critical dimension, etching an underlying interlayer

dielectric in unmasked areas to leave adjacent first and second trenches having a width corresponding to the critical dimension, and then filling the first and second trenches with interconnect metallization to form first and second metal lines, a method for reducing variation in parasitic capacitance between the metal lines attributable to a variation in critical dimension, the method comprising the steps of:

determining a range of critical dimensions exhibited by a photolithography process; and

simulating variation in parasitic capacitance over the critical dimension range by determining the extent of penetration of an overlying third metal line into an inter-line region between the metal lines, a width of the inter-line region determined by a thickness of the conformal middle interlayer dielectric and by the critical dimension, such that penetration of the third metal line elevates parasitic capacitance while reducing parasitic capacitance variation over the critical dimension range.

11. An interconnect structure comprising:

a lower interlayer dielectric positioned over a semiconductor workpiece;

a first metal line formed over the lower interlayer dielectric;

a second metal line formed over the lower interlayer dielectric and separated from the first metal line by an inter-line region;

a middle interlayer dielectric covering the first and second metal lines and the lower interlayer dielectric in the inter-line region; and

a third metal line projecting between the first and second metal lines and separated from the first and second metal lines by the middle interlayer dielectric, the third metal line in electrical communication with one of the first and the second metal lines.

12. An interconnect according to claim 11 wherein the interconnect metallization layer has a thickness, and wherein a thickness of the middle interlayer dielectric is approximately 20% that of the interconnect metallization

13. An interconnect according to claim 11 wherein the interconnect metallization layer is substantially composed of copper.

14. An interconnect according to claim 11 wherein the interconnect metallization layer is substantially composed of aluminum.

15. An interconnect according to claim 11 wherein the middle interlayer dielectric is composed of a dielectric material selected from the group consisting of chemical vapor deposited oxide, borophosphosilicate glass, and tetraethylorthosilicate.